The High Voltage/High Power FET (HiVP[1])

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ABSTRACT — **A new device configuration is presented: The High-Voltage/High-Power device (HiVP). This original configuration can dramatically improve the power and decrease the complexity of designing power amplifiers, leading to low cost and higher power. The HiVP uses a new concept, never achieved before, to simultaneously bias a semiconductor device at high voltage while maintaining an optimum output matching impedance close to 50 Ohms. The concept could be applied to many device technologies such as the GaAs MESFET, HEMT, and the Silicon MOSFET, to combine the power of several devices to achieve higher power output over broader bandwidth.**

I. INTRODUCTION

The HiVP is an original device configuration conceived to address two fundamental problems limiting the usefulness of power semiconductor devices such as the GaAs MESFET, HEMT, PHEMT and HBT devices. These two problems are low operating voltage (usually less than 10V) and high matching losses due to low optimum output matching impedance. A typical optimum impedance for a 10mm power MESFET device (i.e. 3Watt output power) is close to 5 Ohms which is difficult to transform to 50 Ohms. The HiVP on the other hand is a High Voltage, High impedance and High power device configuration in which several large MESFET devices (or other type of devices) are connected DC and RF in series to achieve the following:

1- Bias the HiVP at high voltage.
2- Increase the optimum output impedance from very low value to a value close to 50 Ohm which is an optimum impedance for all planar transmission lines.
3- Use the HiVP for power combining. As several devices are connected together in the HiVP configuration the output power of that configuration is the combined sum of all powers available from each individual device which makes the HiVP configuration an attractive power combiner.
4- Raise the power limits of GaAs devices. Due to the simplicity of the HiVP device configuration very broadband performance can be achieved which cannot be achieved using conventional devices.

Although the High Voltage FET idea has been known in the microwave industry for almost 16 years [1]-[3], the RF power in each of the devices are independent of each other. In order to combine all the RF power of the individual devices that are DC connected in series an external power combiner had to be used. The HiVP device is a different concept where the power is combined internally with minimum or no RF circuitry needed to combine the power output from all the GaAs devices. This HiVP configuration offers an original way to improve the power and simplify the design of power GaAs devices, moreover, the same concept can be applied to other transistors such as Silicon Bipolar or Silicon MOSFET devices to obtain extremely high power in the Kilowatt range with minimum matching circuitry.

Section II describes the HiVP concept. Sections III & IV illustrate the implementation of the concept in hybrid and MMIC format respectively.

II. HIVP CONFIGURATION

Figure 1 illustrates the conventional High Voltage FET configuration where several GaAs FETs are connected in series to raise the bias voltage from around 6 - 10Volts to around 24 - 40 Volts which is a better choice for most communications and satellite systems. Notice in Figure 1 that the capacitors connected to the sources of the series FETs are used to provide RF ground to each device and to enable a conventional parallel combining circuitry to be used to combine the output power of all the devices.

[1] United States Patent No. 6,137,367

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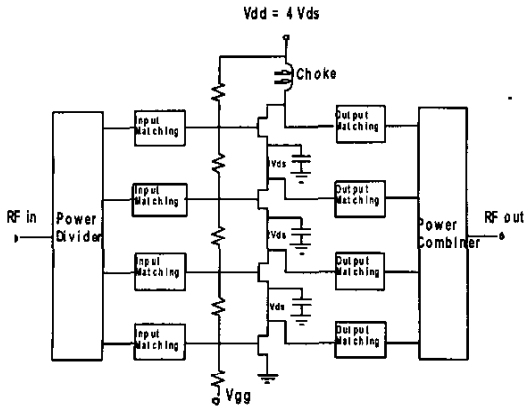

Figure 1: Conventional High Voltage FET

The HiVP configuraton is shown in Figure 2 which illustrates the HiVP configuration for MESFETs. The DC connections of the HiVP are similar to High Voltage FET and the gate resistors are designed to ensure that the DC voltage between drain and source of each device are exactly the same.

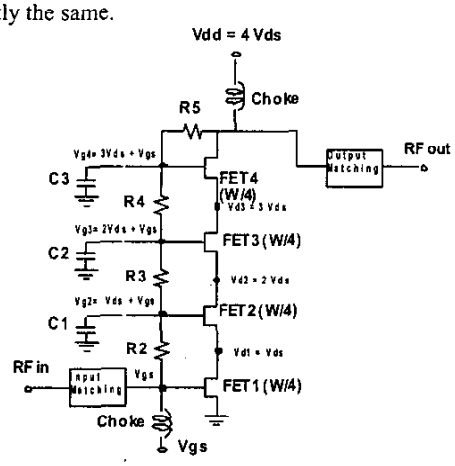

Figure 2: A 4-Cell HiVP Configuration

One important difference between the High Voltage FET and the HiVP is the resistor on the feedback path from the drain of the top FET to its gate. This feedback resistor is absolutely necessary to allow maximum voltage swing on the output resulting in maximum power. Without this feedback arrangement and under RF power the gate voltages of all the series FETs would remain constant while the source of each FET would be varying with a voltage swing depending on the input power level resulting in early device breakdown due to the gate-source limited allowable voltage swing resulting in low power output. On the contrary with feedback the gate voltages swing up and down with the drain voltage of the top FET and hence they closely track the source voltages of each individual FET. If the HiVP is considered a MESFET with the gate of the first cell as the input and the drain of the top cell as the output it is found that it has DC I-V characteristics similar to each FET cell but with the drain voltage scale multiplied by the number of series devices. This statement is not correct for the High Voltage FET.

Another important feature of this configuration is the addition of capacitors between the gates of the floating FETs and ground. These capacitors play a very important role in adjusting the impedance level seen by the drains of each individual device. This impedance adjustment is important since the optimum power from each device is delivered only when the drain of the device is matched to the optimum impedance. Assume that Z_{opt} is the optimum impedance needed at the drain source terminal of each FET cell. Consequently for the HiVP configuration in Figure 2, the optimum impedance at the drain of FET1 should be Z_{opt} at the drain of FET2 it should be 2 Z_{opt} and at the drain of FET4 it should be 4 Z_{opt}. Capacitors C1, C2 and C3 are instrumental in adjusting these impedance levels. The impedance at the source input of each FET is approximately equal to:

$$Z_{source} \cong 1/g_m * (C_{gs}+C_{shunt})/C_{shunt} \quad (1)$$

Where Z_{source} is equal to the source input impedance of each FET

g_m is the FET cell transconductance

C_{gs} is the gate to source FET cell capacitance

C_{shunt} is the shunt capacitance between gate and ground

The HiVP device configuration has several advantages over conventional parallel power combining:

1- High positive voltage can be used to bias the device up to V_{ds} x N where V_{ds} is the optimum cell drain-to-source bias and N is the number of cells.
2- Lower current (1/N factor) for same FET periphery and same power.
3- Higher optimum impedance for maximum power by a factor N x N compared to a regular FET with the same power.
4- Higher power can be achieved using the HiVP compared to conventional designs.
5- Simpler and lower cost matching networks can be implemented for the input and output.
6- The HiVP concept can easily be implemented with other technologies such PHEMT or Silicon devices.

7- High power levels could be achieved by applying the HiVP concept to Silicon devices.

III. Implementation Of A 2-Cell Hybrid HiVP

To prove the concept, a 2-Cell HiVP circuit was implemented, using 2 FET with 7.2mm per cell, on BeO substrate to allow heat dissipation while keeping the device floating above the ground. The output power at 1dB compression from the 2-cell HiVP was measured to be 37dBm. The power density is calculated to be 0.35W/mm. These results are limited to frequencies below 1GHz due to the substrate parasitics. Fig. 3 shows the layout of the hybrid circuit.

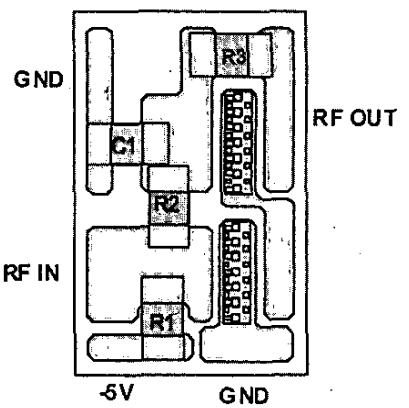

Figure 3: Hybrid Layout of 2-cell HiVP

IV. Implementation Of A 2-Cell & 4-Cell MMIC HiVP

The HiVP was implemented in MMIC format. Fig. 4 shows the layout of a 2-cell and a 4-cell MMIC devices. The power MMIC process used in the circuits yields 0.35W/mm with around 45% efficiency at 1dB compression point. Several 2-cell circuits were tested with each cell having a 2 mm device per cell.

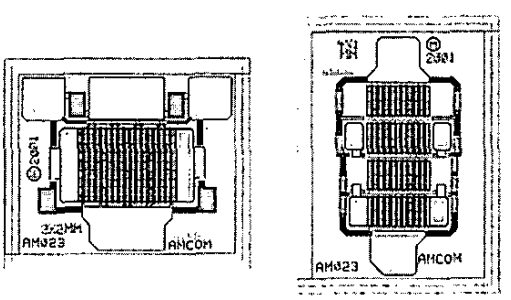

Figure 4: Layout of 2-Cell & 4-Cell HiVP Circuits

Fig. 5 shows the gain and input/output return loss of the device without any matching network. Fig. 6 shows the measured Pout versus Pin, gain and efficiency at 3.5GHz with a tuner on the output for optimum results. The P1dB is 31.5dBm which yields 0.35W/mm with an efficiency of 42% at 1dB compression. This power comparable to the power obtained from a 4mm device with almost same efficiency. Note that the efficiency is few percentage points lower than conventional design due to power dissipation in the bias resistors. Fig. 7 shows the results of the intermodulation (IMD) data at 3.5GHz. The IMD data shows excellent linearity due to the strong negative feedback effect in the HiVP configuration. The IP3 is around 46dBm which is 14dB higher than the 1dB point of the device. The IP5 is around 55dBm. The value of IP3 & IP5 is higher for the HiVP than the IP3 & IP5 of a device with comparable power. The improvement is caused by the feedback effect of the HiVP configuration.

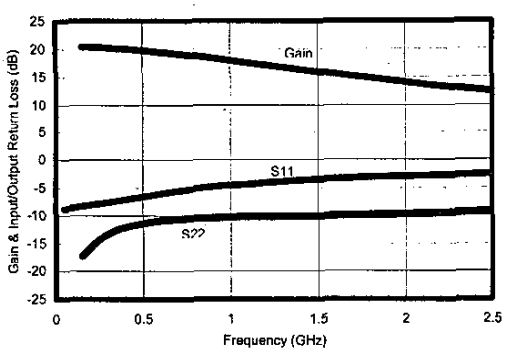

Figure 5: Gain and Input/Output Return Loss measurements (Vdd = 14V, Idd=200mA)

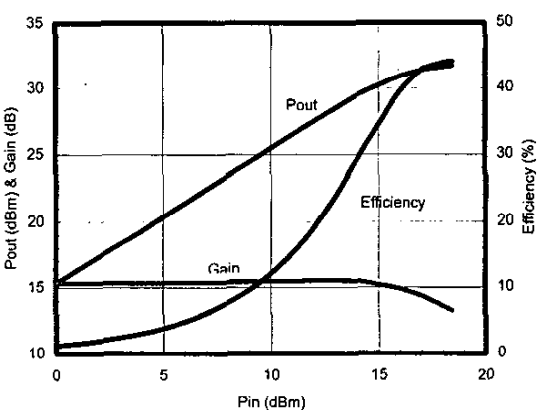

Figure 6: Power measurements at 3.5GHz at optimum load (Vdd = 14V, Idd=200mA)

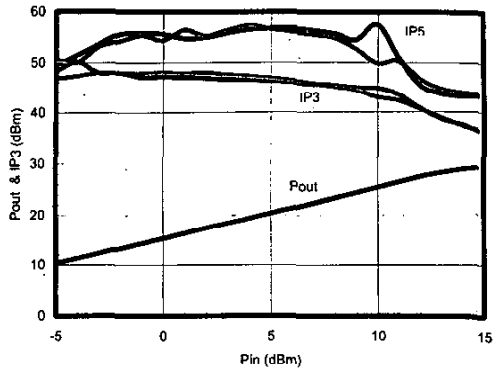

Figure 7: Pout, IP3 & IP5 measurements at 3.5GHz at optimum load (Vdd = 14V, Idd=200mA)

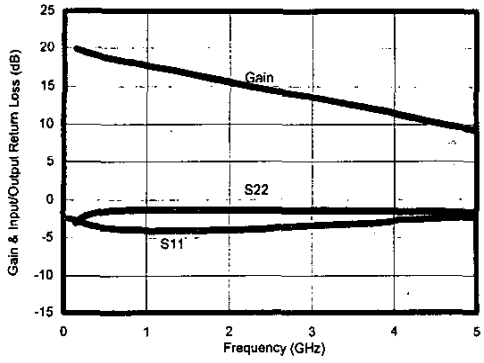

Figure 8: Gain and Input/Output Return Loss measurements (Vdd = 28V, Idd=100mA)

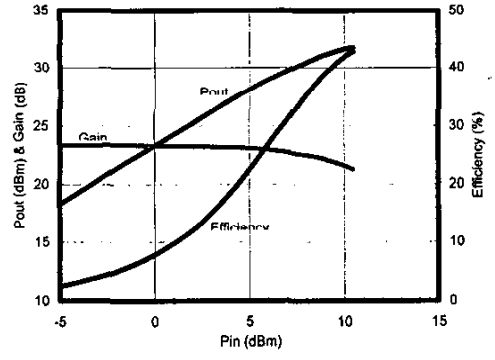

Figure 9: Power measurements at 1GHz at optimum load (Vdd = 28V, Idd=100mA)

A 4-cell device with 1mm per cell was measured. The data is summarized in Figs. 8, 9 and 10. At optimum power match, the 4-cell output power at 1dB compression is around 31.5dBm and the efficiency is 35%. The power is the same as the P1dB obtained from a 4mm device using the conventional approach.

Figure 10: Power measurements at 3.5GHz at optimum load (Vdd = 28V, Idd=100mA)

V. Conclusion

In summary, we have described a novel device/circuit configuration which can be applied to a variety of devices such as the GaAs MESFET, HEMT, P-HEMT and the Silicon MODFET to simultaneously achieve power levels not possible using conventional designs, combine the output powers of several FET cells and to bias the entire circuit at higher voltages than that possible with a single device. All of the above can be implemented in a simple and straightforward technique using our configuration the HiVP device concept.

Acknowledgement

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